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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	KIBROM K. GEBRESILASSIE	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,5 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4, 5, and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/09/2009 has been entered.

2. Claims 4, 5, and 12 are presented for examination.

Response to Arguments

3. Applicants submitted replacement drawings to overcome the objection and therefore they are considered and are entered.

4. Applicant's argument relating to 101 rejection is persuasive and therefore the rejection is withdrawn.

5. Applicant's argument relating to 102(f) rejection is not persuasive.

a. Applicant argues:

> "Assignee respectfully traverses the rejection and submits that the foregoing Specification 0006 does not teach "a second circuitry configured to realize and verify the second system on another chip *while the first circuit verifies the first system on chip,* the second circuitry directly connected to the first circuitry". Clearly, by configuring the second circuitry to "realize and verify the second system chip *while the first circuit verifies the first system on a chip",* a transformation of the emulator occurs."

The above recited limitations such as "first circuitry" and "second circuitry" are inherent to the conventional hardware emulator because it is a device with a large amount of logic and other circuitry with highly configurable connections, further, a script checks the capacity of the hardware emulator to determine

whether the hardware emulator has sufficient logic and circuitry to realize the design…(See: [0006]). Therefore, the above recited limitations are still read on the conventional hardware emulator.

6. Applicant's argument relating to art rejection is not persuasive.

b. Applicant argues:

> "Claim 4 was also rejected under 35 U.S.C. § 102(e) as being anticipated by Rohlfleisch. Examiner has made citation to Rohlfleisch [0039]. However, Rohlfeisch [0039] states that "Advantageously, the emulator circuits 104, 108 and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate, and/or debug the processor core 102 and/or the other core 106 using the emulation interface circuit 110." Note, however that "emulator circuits 104, 108" are in fact, two emulator circuits. In contrast, Assignee claims "a hardware emulator for verifying a first system on a chip and a second system on another chip" - noting the use of the singular context in the claim."

Rohlfeisch et al discloses two emulator circuitries which are equivalent to "first circuitry" and "second circuitry" to verify the processor core 102 (i.e. first system on a chip) and Other Core 106 (i.e. second system on another chip) (See: par [0026]-[0028], [0032]-[0033]).

c. Applicant argues:

> "Additionally, Rohlfleisch also does not teach "a hardware emulator for verifying a first system on a chip and a second system on another chip, said hardware emulator comprising: a first circuitry configured to realize and verify the first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry; and a second circuitry configured to realize and verify the second system on another chip while the first circuit verifies the first system on chip, the second circuitry directly connected to the first circuitry."

Applicant's arguments amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

The prior art of reference discloses, for example, *the emulator circuit 104, 108 (i.e. first and second circuitries) and the emulator interface circuit 110 permit an SOC designer or programmer to test, evaluate and/or debug the processor core 102 (i.e. verify the first system on a chip) and/or the other core 106 (i.e. verify the second system on another chip) using the emulation interface circuit 110* (See: par [0039]).

Further, the emulator circuit 104, 108 (i.e. first and second circuitries) are directly connected through the emulator interface circuit 110 as illustrated in Figure 1.

Applicants Admission

7. Applicant's disclosure states as follows:

> **[0006]** Many chip-makers now use a device called a hardware emulator to verify SOCs. A hardware emulator is a device with large amounts of logic and other circuitry with
>
> highly configurable connections. The connections can be configured so as to realize the design of the SOC. The design is usually described in a data structure. A script checks the capacity of the hardware emulator to determine whether the hardware emulator has sufficient logic and circuitry to realize the design described in the data structure. If the hardware emulator has sufficient capacity to realize the design described in the data structure, the script places the data structure in a top wrapper. The top wrapper parses the data structure describing the design and configures the hardware emulator to realize the design.

Compare to claimed invention:

[0023] FIGURE 2 is a block diagram of a hardware emulator configured in accordance with an embodiment of the present invention. The hardware emulator 200 comprises a sea of logic and other circuitry 205. The sea of logic and other circuitry 205 is configurable to realize a vast number of integrated circuits. The sea of logic and other circuitry can be divided into a plurality of portions 210.

[0026] The emulator 200 of FIGURE 2 can be configured by a computer system configured generally as described in FIGURE 3. An SOCs, SOC1...SOCn can be described in a data structure in a file. The file is parsed by a script. A script is a plurality of executable instructions stored in the memory of the computer system, or a removable memory, that parses the data structures, checks the capacity of the emulator 200, and creates another file, known as a top wrapper. The top wrapper is provided to the emulator and configures the emulator 200 in accordance with the SOCs described in the data structure.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (f) he did not himself invent the subject matter sought to be patented.

9. Claims 4, 5, and 12 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter.

d. Applicant's admission establishes that applicant has invented a system of using a hardware emulator for verifying a plurality of systems of the prior art. Applicants have not disclosed inventing a hardware emulator system. As such, any claims directed to a system that facilities this system must be regarded as being invented by another.

e. These rejection may be overcome by evidence that applicant has somehow transformed the hardware emulator system of the prior art by some specialization. As currently disclosed, however, applicants' system of verifying using a hardware emulator merely uses the existing feature of the prior art.

f. Evidence that hardware emulator anticipates the invention of claims 4, and 5 is found in applicant's admission as explicitly recited in the disclosure of the invention.

10. Claims 4, 5 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Publication No. 2004/0019827 issued to Rohfleisch et al.

a. As per Claims 1-3, Canceled.

b. As per Claim 4, Rohfleisch et al discloses a system for verifying a plurality of systems on a plurality of chips (such as *…SOC designer to test or evaluate and/or debug….*;See: [0039]), said system comprising:

a hardware emulator for verifying a first system on a chip and a second system on another chip (such as *…to test or evaluate and/or debug the processor core 102 (i.e. first system on another chip) and/or the other core (i.e.*

*second system on chip) using the emulation interface circuitry...*See: [0039]) said hardware emulator comprising:

a first circuitry configured to realize and verify the a first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry system on the chip (such as *…to test or evaluate and/or debug the processor core 102 (i.e. second system on another chip*) *and/or the other core using the emulation interface circuitry...*See: [0039]); and

a second circuitry configured to realize and verify the a second system on another chip while the first circuit verifies verifying the first system on chip, the second circuitry directly connected to the first circuitry (such as *…to test or evaluate and/or debug the processor core 102 and/or the other core (i.e. second system on another chip*) *using the emulation interface circuitry...*See: [0039]).

c. As per Claim 5, Rohfleisch et al discloses the system of claim 4, wherein the hardware emulator further comprises:

a first interface operable connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry (such as *…to test or evaluate and/or debug the processor core 102 and/or the other core using the emulation interface circuitry...*See: [0039]); and

a second interface operable connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (such as *…to test or evaluate and/or debug the*

*processor core 102 and/or the other core using the emulation interface circuitry...*See: [0039]).

d. As per Claim 6-11, Cancelled.

e. As per Claim 12, Rohfleisch et al discloses the system of claim 4, wherein verifying the plurality of systems further comprises detecting errors in the plurality of systems (such as…*debugging of programs and operation of systems-on-a-chip…*; See: Abstract).

11. **Support for Amendments and Newly Added Claims**, Applicants are respectfully requested, in the event of an amendment to claims or submission of new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution. MPEP 714.02 recites: "Applicant should also specifically point out the support for any amendments made to the disclosure. See MPEP § 2163.06. An amendment which does not comply with the provisions of 37 CFR 1.121(b), (c), (d), and (h) may be held not fully responsive. See MPEP § 714." Amendments not pointing to specific support in the disclosure may be deemed as not complying with provisions of 37 C.F.R. 1.131(b), (c), (d), and (h) and therefore held not fully responsive. Generic statements such as "Applicants believe no new matter has been introduced" may be deemed insufficient.

12. **Requests for Interview**, In accordance with 37 CFR 1.133(a)(3), requests for interview must be made in advance. Interview requests are to be made by telephone (571-272-8634) call or FAX (571-273-8634). Applicants must provide a detailed agenda

as to what will be discussed (generic statement such as "discuss §102 rejection" or "discuss rejections of claims 1-3" may be denied interview). The detail agenda along with any proposed amendments is to be written on a PTOL-413A or a custom form and should be faxed (or emailed, subject to MPEP 713.01.I / MPEP 502.03) to the Examiner at least 3 days prior to the scheduled interview.

Interview requests submitted within amendments may be denied because the Examiner was not notified, in advance, of the Applicant Initiated Interview Request and due to time constraints may not be able to review the interview request to prior to the mailing of the next Office Action

Conclusion

13. All claims are rejected.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KIBROM K. GEBRESILASSIE whose telephone number is (571)272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

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